CLAIMS

What is claimed is:

1. A protective structure for blocking the propagation of defects generated in a semiconductor device, the structure comprising:

a deep trench isolation formed between a memory storage region of the semiconductor device and a logic circuit region of the semiconductor device, said deep trench isolation being filled with an insulative material;

wherein said deep trench isolation prevents the propagation of crystal defects generated in said logic circuit region from propagating into said memory storage region.

2. The structure of claim 1, wherein said deep trench isolation is formed beneath a shallow trench isolation, said shallow trench isolation for electrically isolating devices contained in said memory storage region from devices contained in said logic circuit region.

3. The structure of claim 1, further comprising a plurality of deep trench isolations surrounding said memory storage region.

4. The structure of claim 3, wherein said plurality of deep trench isolations further comprise:

an inner perimeter and an outer perimeter, wherein individual deep trench isolations included in said outer perimeter are disposed adjacent to gaps in between individual deep trench isolations included in said inner perimeter.

5. The structure of claim 1, wherein said memory storage region comprises a DRAM array region.

6. The structure of claim 5, wherein said DRAM array region includes a plurality of deep trench storage capacitors.

7. The structure of claim 6, wherein said logic circuit region further includes:

a plurality of CMOS devices; and

a high dose impurity layer implanted within a substrate of said logic circuit region, said high dose impurity layer used to inhibit parasitic bipolar transistor action between said plurality of CMOS devices.

8. An embedded DRAM (eDRAM) device, comprising:

a logic circuit region;

a memory storage region embedded within said logic circuit region;

a shallow trench isolation for electrically insulating devices included within said memory storage region from devices included within said logic circuit region; and

a deep trench isolation, formed underneath said shallow trench isolation, said deep trench isolation for preventing the propagation of crystal defects generated in said logic circuit region from propagating into said memory storage region.

9. The eDRAM device of claim 8, wherein said shallow trench isolation surrounds said memory storage region.

10. The eDRAM device of claim 9, further comprising a plurality of deep trench isolations surrounding said memory storage region.

11. The eDRAM device of claim 10, wherein said plurality of deep trench isolations further comprise:

an inner perimeter and an outer perimeter, wherein individual deep trench isolations included in said outer perimeter are disposed adjacent to gaps in between individual deep trench isolations included in said inner perimeter.

12. The eDRAM device of claim 11, wherein said memory storage region includes a plurality of deep trench storage capacitors.

13. The eDRAM device of claim 12, wherein said logic circuit region further includes:

a plurality of CMOS devices; and

a high dose impurity layer implanted within a substrate of said logic circuit region, said high dose impurity layer used to inhibit parasitic bipolar transistor action between said plurality of CMOS devices.

14. A method for blocking the propagation of defects generated in a semiconductor device, the method comprising:

forming a deep trench isolation formed between a memory storage region of the semiconductor device and a logic circuit region of the semiconductor device; said deep trench isolation being filled with an insulative material;

wherein said deep trench isolation prevents the propagation of crystal defects generated in said logic circuit region from propagating into said memory storage region.

15. The method of claim 14, wherein said deep trench isolation is formed beneath a shallow trench isolation, said shallow trench isolation for electrically isolating devices contained in said memory storage region from devices contained in said logic circuit region.

16. The method of claim 14, further comprising forming a plurality of deep trench isolations to surround said memory storage region.

17. The method of claim 16, further comprising:

configuring said deep trench isolations to form an inner perimeter and an outer perimeter, wherein individual deep trench isolations included in said outer perimeter are disposed adjacent to gaps in between individual deep trench isolations included in said inner perimeter.

18. The method of claim 14, wherein said memory storage region comprises a DRAM array region.

19. The method of claim 18, wherein said DRAM array region includes a plurality of deep trench storage capacitors.

20. The method of claim 19, wherein said logic circuit region further includes:

a plurality of CMOS devices; and

a high dose impurity layer implanted within a substrate of said logic circuit region, said high dose impurity layer used to inhibit parasitic bipolar transistor action between said plurality of CMOS devices.